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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/725,762	11/30/2000	Robert J. Donaghey	99-463A	1627

32127 7590 10/26/2004

VERIZON CORPORATE SERVICES GROUP INC.
C/O CHRISTIAN R. ANDERSEN
600 HIDDEN RIDGE DRIVE
MAILCODE HQE03H14
IRVING, TX 75038

EXAMINER	
PHAN, MAN U	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 10/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/725,762	DONAGHEY ET AL.	
	Examiner	Art Unit	
	Man Phan	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,9-12,14-16,18 and 19* is/are rejected.

7)☒ Claim(s) *4,8,13 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/30/2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/07/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The application of Rehn et al. for a "Systems and methods for implementing global virtual circuits in packet-switched networks" filed 11/30/2000 has been examined. Claims 1-19 are pending in the application.

Claim Rejections - 35 USC ' 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 1038 and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Opalka et al. (US#6,259,699) in view of Shue et al. (US#6,222,845).

With respect to claims 5-7, Opalka et al. (US#6,259,699) discloses a novel system and method for routing and forwarding of information in packet switching network, according to the essential features of the claims. Opalka et al. (US#6,259,699) discloses in Figs. 4 & 14 block diagrams illustrated the novel networking architecture and technique for routing packets or frames information across a common switch fabric using forwarding engine with common algorithm for forwarding based on control information contained in the frame. An ATM switch makes forwarding decision based on control information provided in the ATM header, by looking at a forwarding table based on VPI/VCI numbers, Fig. 1. The forwarding table is typically indexed by physical port number, i.e. an incoming cell with a VPI/VCI on ingress port N gets mapped to an egress port M with a new VPI/VCI pair. The table is managed by software elsewhere in the system. All cells, no matter what the ATM Adaptation Layer (AALx), have the same structure, so that if ATM switches can forward one AAL type, they can forward any type (Col. 6, lines 23 plus). As packets enter the interface card, the packet header is examined by a Header Lookup and Forwarding Engine module 14 while the data is sent to the NeoN data switch 4. The Ingress Forwarding Engine makes a forwarding decision about the QoS and the destination interface card based on the incoming packet header. The packet-based forwarding engine decides the egress port and associates a VCI number for cells of that packet. The Forwarding Engine 14 also gathers all information regarding the data packet, like NeoN Switch address, Packet QoS, Egress Header Translation information, and sends it across to the egress interface card. This information is carried as a control packet to

the egress port through the small non-blocking control data switch 8 to the Egress QoS module 6, which will queue data as per the control packet and send it to the module listed PHY at the egress. If the packet were to egress to a cell interface, the packet will be segmented, then header translated and shaped before it leaves the interface (Col. 14; lines 22 plus). Opalka further teaches in Fig. 11 a traditional Packet Switch with native packet interface cards. Packets are forwarded to the Forwarding Engine via the physical interface. The Forwarding Engine makes a routing decision based on some algorithm and the header of the packet (*connection information*). Once the egress port is decided, the packet travels to the egress via the Packet Switch, which could be designed in one of many ways (e.g. N by N busses, large central memory pool, etc.). On egress, the packets end up on different traffic priority Queues. These Queues are responsible for prioritizing traffic and bandwidth management (Col. 12; lines 17 plus).

However, Opalka et al. (US#6,259,699) does not expressly disclose the determining at least one virtual circuit path to at least one switch in the network. In the same field of endeavor, Shue et al. (US#6,222,845) discloses a network for transferring information among a plurality of digital devices includes a plurality of switching nodes interconnected by communication links. Each of the digital devices is connected to one of the switching nodes over additional ones of communication links. Each communication link transfers information in a predetermined one of a plurality of types of communications services, with the network including at least one communication link of each service type. The digital devices and switching nodes transfer information through the network over virtual circuits, with each virtual circuit extending from one digital device, as an originating digital device, to another

digital device, as a terminating digital device. Each virtual circuit defines a unitary virtual circuit path extending through at least one switching node over a plurality of the communication links without regard to the service type of the ones of the communication links included in the virtual circuit path (See Fig. 6, Col. 3, lines 22 plus).

Regarding claims 1-3, they are method claims corresponding to the apparatus claims 5-7 above. Therefore, claims 1-3 are analyzed and rejected as previously discussed with respect to claims 5-7.

Regarding claim 7, this claim differs from claims Opalka in view of Shue in that the claim recited a computer program product for performing the same basis of steps and apparatus of the prior arts as discussed in the rejection of claims 1-3 and 5-7 above. It would have been obvious to a person of ordinary skill in the art to implement a computer program product in Opalka in view of Shue for performing the steps and apparatus as recited in the claims with the motivation being to provide the efficient enhancement to the throughput of the multi hop virtual circuit paths in switching network, and easy to maintenance, upgrade.

One skilled in the art would have recognized the need for effectively and efficiently routing and forwarding of information in packet switching network, and would have applied Shue's teaching in the process of forwarding the virtual circuit path information block to the next switching node into Opalka's novel use of the forwarding and routing information in packet switched communication. Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to apply Shue's system and method for providing unitary virtual circuit in digital network having communication links of diverse service types into Opalka's system architecture for and method of processing packets

and/or cells in a common switch with the motivation being to provide a method and apparatus for routing and forwarding of information in packet switching network.

4. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Opalka et al. (US#6,259,699) in view of Shue et al. (US#6,222,845) as applied to the claims above, and further in view of vatuone (US#5,621,721).

With respect to claims 14-16 and 19, Opalka et al. (US#6,259,699) and Shue et al. (US#6,222,845) disclose the claims as discussed in paragraph 3 above. However, these claims differ from the claims above in that the claims require the processor updates information pertaining to locations and paths to switches in the network based on the received connection information. In the same field of endeavor, Vatuone (US#5,621,721) discloses in Fig. 2 a block diagram illustrated a communication node comprises a main processor unit, in which the maintenance of database consistency among the nodes of a communication network. Typically, each communication node in such a network maintains a set of routing databases that specify the routing of all virtual circuit paths through the communication links and communication nodes of the network. In addition, such routing databases may specify the network resources allocated to the virtual circuits. Typically, the main processor in such a communication node maintains and updates a main routing database while the auxiliary processor maintains and updates an auxiliary routing database that reflects the exact contents of the main routing database. Such an updated auxiliary database enables rapid switchover from the main processor to the auxiliary processor upon a failure in the main processor or main processor software.

A virtual circuit is typically established in such a communication network by transferring routing messages to each communication node. The routing messages usually specify a physical path through the communication network and a corresponding set of communication resources for the virtual circuit. The routing messages enable the main processor in each communication node to update the internal main routing database. In addition, each main processor typically causes the corresponding auxiliary processor to update the internal auxiliary routing database to reflect the new routing information (Col. 1, lines 46 plus and col. 8, lines 15 plus).

Regarding claims 10-12, they are method claims corresponding to the apparatus claims 14-16 above. Therefore, claims 10-12 are analyzed and rejected as previously discussed with respect to claims 14-16.

Regarding claim 18, this claim differs from claims Opalka in view of Shue in that the claim recited a computer program product for performing the same basis of steps and apparatus of the prior arts as discussed in the rejection of claims 10-12 and 14-16, 19 above. It would have been obvious to a person of ordinary skill in the art to implement a computer program product in Opalka in view of Shue and Vatuone for performing the steps and apparatus as recited in the claims with the motivation being to provide the efficient enhancement to the throughput of the multi hop virtual circuit paths in switching network, and easy to maintenance, upgrade.

One skilled in the art would have recognized the need for effectively and efficiently routing and forwarding of information in packet switching network, and would have applied Vatuone's novel use of the maintaining and updating a main routing database information; Shue's teaching in the process of forwarding the virtual circuit path information block to the next switching node into Opalka's novel use of the forwarding and routing information in packet switched communication. Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to apply Vatuone's maintaining database integrity throughout a communication network, and Shue's system and method for providing unitary virtual circuit in digital network having communication links of diverse service types into Opalka's system architecture for and method of processing packets and/or cells in a common switch with the motivation being to provide a method and apparatus for routing and forwarding of information in packet switching network.

Allowable Subject Matter

5. Claims 4, 8, 13, 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The closest prior art of record fails to disclose or suggest wherein each outgoing circuit identifier (VCI_{out}) for VC table entry b + e, for each value of h, is determined by: $VCI_{out} = 2 + 4^1 + \ldots + 4^{h-2} + ((e-b) \bmod 4^{h-2})$; where $b = 2 + 4^1 + \ldots + 4^{h-1}$ and $e < 4^h$, as specifically recited in the claims 4, 8, 13, 17.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The Chen (US#6,765,908) is cited to show the system and method for transferring packets in a connectionless network.

The Garcia-Luna-Aceves et al. (US#6,683,865) is cited to show the system for routing and switching in computer networks

The Buckman et al. (US#2002/0188732) is cited to show the system and method for allocating bandwidth across a network.

The Schibler et al. (US#5,528,592) is cited to show the method and apparatus for route processing ATM cells.

The Gupta (US#6,278,714) is cited to show the efficient hardware implementation of virtual circuit bunching.

The Iwata (US#5,473,603) is cited to show the signaling system utilizing source routing information in a packet network.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Phan whose telephone number is (571) 272-3149.

The examiner can normally be reached on Mon - Fri from 6:00 to 3:00 EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu, can

be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2600.

8. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

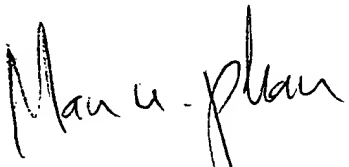
or faxed to: (703) 305-9051, (for formal communications intended for entry)

Or: (703) 305-3988 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2021 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Mphan

10/21/2004.



MAN U. PHAN
PRIMARY EXAMINER